RAJEEV GANDHI MEMORIAL COLLEGE OF ENGINEERING AND TECHNOLOGY
(AUTONOMOUS)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

CO-PO Mapping of Project in the area of Application of VLSI Design

Title of the Project: Design of Dual Channel Multiplier

Area of the Project: VLSI Design

Methodology: Simulation

Name of the Supervisor: Dr. R. HANUMA NAIK M.Tech, Ph.D.,

Name of the Students:

N. VENKATA MADHURI (19091A04Q6)
S. K. BENARJEE (19091A0419)
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Abstract:

In this project, A dual-channel multiplier for piecewise-polynomial function of energy efficient and power efficient is proposed for 3-D graphics applications. It Compensates the complex multipliers by using DCM where it reduces the hardware complexity. DCM scheme performs complex functions with power-efficient and area efficient approach. it reduces the hardware computational effort in the piecewise polynomial approximation with uniform or non-uniform segmentation. The performance of the evaluation process is highly dependent on the design of the multiplication and squaring structure. A novel hardware implementation for polynomial evaluation is presented. The proposed approach compensates the complex multipliers by using DCM which reduces the hardware complexity. The DCM scheme performs complex functions with power efficient and area-efficient approach. The multiplier reduces the hardware computational effort in the piecewise polynomial approximation with uniform or non-uniform segmentation. For large operand input size, a multiplier adder converter and a dedicated radix-4 squaring unit are also proposed. These units achieve the least power consumption compared to previous approaches with large input word size. The above proposed system is designed and developed using VHDL environment.

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Process of CO-PO attainment for Project thesis of IV-year Main Project

Course Outcomes:

1. To identify the problem formulation of the project after literature surveyor study of existing technology
2. To analyze the basic concepts of the project in correlation with theengineering knowledge
3. To apply the concepts of technology with modern tool usage to overcomethe problem.
4. To formulate the solution and to design simulation and prototype of thesolution with the engineering knowledge.

CO-PO Mapping:

CO/P O	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO1 0	PO1 1	PO1 2
CO1	2	-	-	-	-	-	-	-	3	-	-	-
CO2	2	-	2	-	-	-	-	-	3	-	-	-
CO3	2	-	-	-	-	-	-	-	3	-	3	-
CO4	2	-	2	-	2	-	-	-	3	-	3	-

Evaluation:

Projectwork	100	External evaluation	This end viva voce in project work for 100 marks
	25	Internal evaluation	These 25 marks will be based on the performance ofthe student in the project reviews apart from attendance and regularity

Table: Percentage Weightages for each CO:

S.No.	REG	IM 25M	EM grade	TM 125M	EM 100M	%IM	%EM	CO1	CO2	CO3	CO4	N.CO1	N.CO2	N.CO3	N.CO4
1	19091A04Q6	23	10	118	95	92	95	22.56	34.08	18.88	18.88	84.62	102.25	94.44	94.44
2	19091A0419	23	10	117	94	92	94	22.4	33.76	18.72	18.72	84.02	101.29	93.64	93.64
3	19091A04F5	20	10	112	92	80	92	21.12	32.64	17.92	17.92	79.21	97.92	89.64	89.64
4	20095A0414	19	9	109	90	76	90	20.48	31.84	17.44	17.44	76.81	95.52	87.24	87.24

Table: Weightage marks for each CO:

	CO1	CO2	CO3	CO4
Internal	40	20	20	20
External	20	40	20	20
Average	26.66	33.33	19.99	19.99

Table: Percentage Attainment Values for each CO

	Co1		C02		C03		Co4	
Above & Equal 60%	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**
Between 40-60%	**0**	**2**	**0**	**2**	**0**	**2**	**0**	**2**
Below40%	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**
Total students	**4**		**4**		**4**		**4**	
Attainment value		**3.00**		**3.00**		**3.00**		**3.00**
% of attainment		100.00		100.00		100.00		100.00
Attained or not (Greater 50% Y, Not Means N		**Y**		**Y**		**Y**		**Y**

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PROJECT REPORT ON

DESIGN OF DUAL CHANNEL MULTIPLIER

Submitted in partial fulfilment of the Requirement for the award of the degree of

BACHELOR OF TECHNOLOGY

IN

ELECTRONICS AND COMMUNICATION ENGINEERING

Submitted by

	Regd. No:
N.Venkata Madhuri	19091A04Q6
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CERTIFICATE

This is to certify that the dissertation entitled "DESIGN OF DUAL CHANNEL MULTIPLIER" is being submitted by N.Venkata Madhuri (19091A04Q6), S.K.Benarjee (19091A0419), N.Ravi kumar (19091A04F5), P.Sai Kumar Naik (20095A0414) under the guidance of Dr.R.Hanuma Naik, Associate Professor for Project of the award of B.Tech Degree in Electronics and Communication Engineering, Rajeev Gandhi Memorial College of Engineering & Technology, Nandyal (Autonomous) (Affiliated to J.N.T.U.A Anantapuramu) is a record of bonafide work carried out by them under our guidance and supervision.

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ABSTRACT

In this project, A dual-channel multiplier for piecewise-polynomial function of energy efficient and power efficient is proposed for 3-D graphics applications. It Compensates the complex multipliers by using DCM where it reduces the hardware complexity. DCM scheme performs complex functions with power-efficient and area efficient approach. it reduces the hardware computational effort in the piecewise polynomial approximation with uniform or nonuniform segmentation. The performance of the evaluation process is highly dependent on the design of the multiplication and squaring structure. A novel hardware implementation for polynomial evaluation is presented. The proposed approach compensates the complex multipliers by using DCM which reduces the hardware complexity. The DCM scheme performs complex functions with power efficient and area-efficient approach. The multiplier reduces the hardware computational effort in the piecewise polynomial approximation with uniform or nonuniform segmentation. For large operand input size, a multiplier adder converter and a dedicated radix-4 squaring unit are also proposed. These units achieve the least power consumption compared to previous approaches with large input word size. The above proposed system is designed and developed using VHDL environment.

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CHAPTER 6
CONCLUSION AND FUTURE SCOPE

6.1 CONCLUSION

The implementation of PWP evaluation in the SFU of the GPUs can be highly improved by boosting the performance of multiplication and squaring unit which are the basic components in the evaluation process. Exploiting the serial/parallel algorithm, an energy efficient DCM is proposed in this paper. Comparisons with the well-known multiplication schemes have demonstrated savings in area, power, and energy. Moreover, for large operand input size, MAC is utilized to replace the traditional parallel multiplier scheme. MAC is proposed to perform the computation of the overall approximated polynomial without the need for multiplication in SFUs. The proposed scheme can implement different functions using simple hardware design. Also, high-speed dedicated squaring unit is proposed. It can be readily applied to any number of bits. PWP function evaluation by MAC is implemented using FPGA

6.2 FUTURE SCOPE

A dual channel multiplier is a type of electronic circuit this multiply two input signals, producing an output signal that is the product of the two inputs. The future scope of such a project largely depends on the specific application and context in which it is being used.

Here are a few potential future scopes for a dual channel multiplier project:

Digital signal processing (DSP) applications: Dual channel multipliers can be used in a wide range of DSP applications, including digital filters, mixers, and modulators. As the demand for DSP continues to grow in various industries, including telecommunications, multimedia, and consumer electronics, the demand for dual channel multipliers is also likely to increase.

Audio and music applications: Dual channel multipliers can be used in audio and music applications to control the gain and amplitude of signals. As the demand for high-quality audio processing and mixing equipment

continues to increase, the use of dual channel multipliers is also likely to grow.

Control systems: Dual channel multipliers can also be used in control systems to adjust the gain of feedback signals. As automation and robotics continue to become more prevalent in various industries, the use of control systems is also likely to increase, leading to a growing demand for dual channel multipliers.

Overall, the future scope of a dual channel multiplier project is likely to be shaped by the continued growth and development of various industries that rely on signal processing, control systems, and other applications that require the manipulation of analog signals.

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